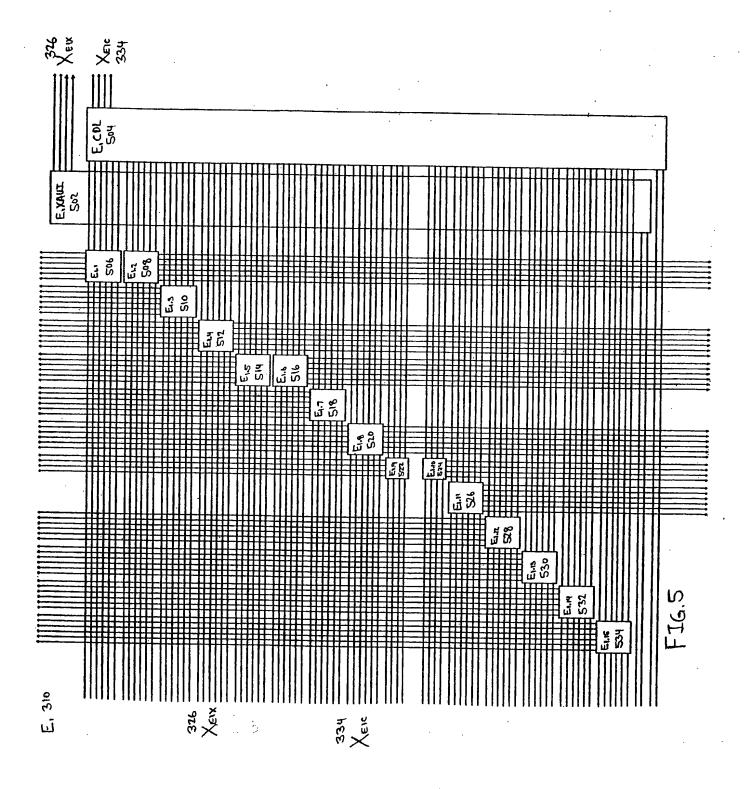


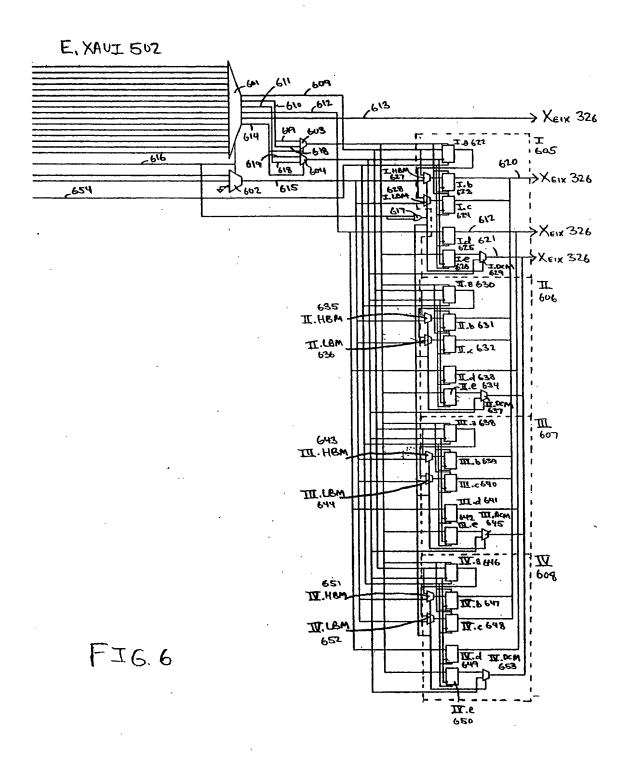
FIG. 4 **TABLE 400**

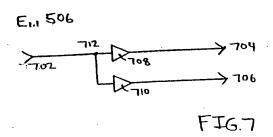
	XAUI Protocol	
Received From Out of Bus	Communicated Within Bus	Transmitted to Out of Bus
40 data bits	40 data bits	80 data bits
4 link bits	4 link bits	
4 lock bits	4 lock bits	••
4 clock bits	4 clock bits	4 clock bits
4 fast clock bits	4 fast clock bits	·
1 CLOCK MODE SELECT bit	1 CLOCK MODE SELECT bit	

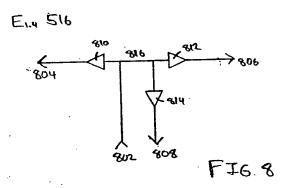
	CDL Protocol	
Received From Out of Bus	Communicated Within Bus	Transmitted to Out of Bus
40 data bits	40 data bits	80 data bits
4 link bits	4 link bits	4 link bits
4 lock bits	4 lock bits	4 lock bits
4 clock bits	4 clock bits	4 clock bits
4 fast clock bits	4 fast clock bits	
1 CLOCK MODE SELECT bit	1 CLOCK MODE SELECT bit	

	XGMII Protocol	
Received From Out of Bus	Communicated Within Bus	Transmitted to Out of Bus
40 data bits	80 data bits	40 data bits
4 lock bits	4 lock bits	
4 clock bits	4 clock bits	4 clock bits
3 MODE SELECT bits		
1 DIFFERENTIAL CLOCK MODE SELECT bit		
	1 CLOCK MODE SELECT bit	
		4 output enable bits









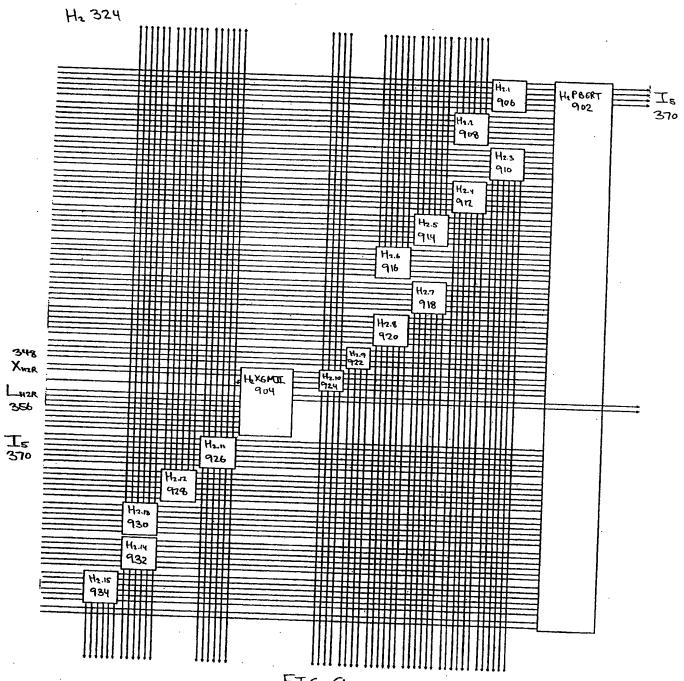
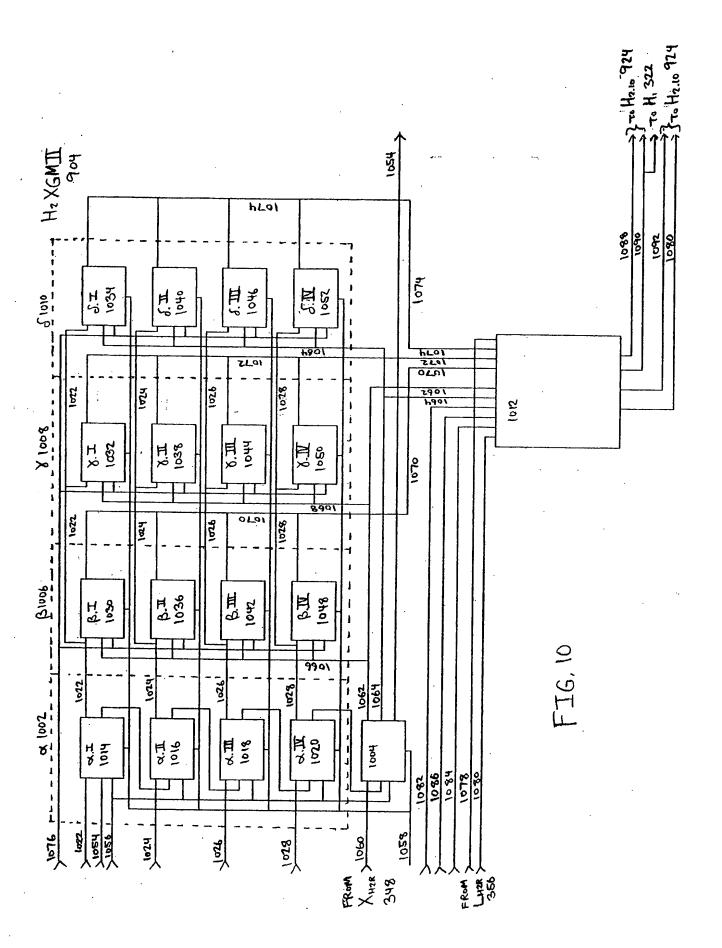
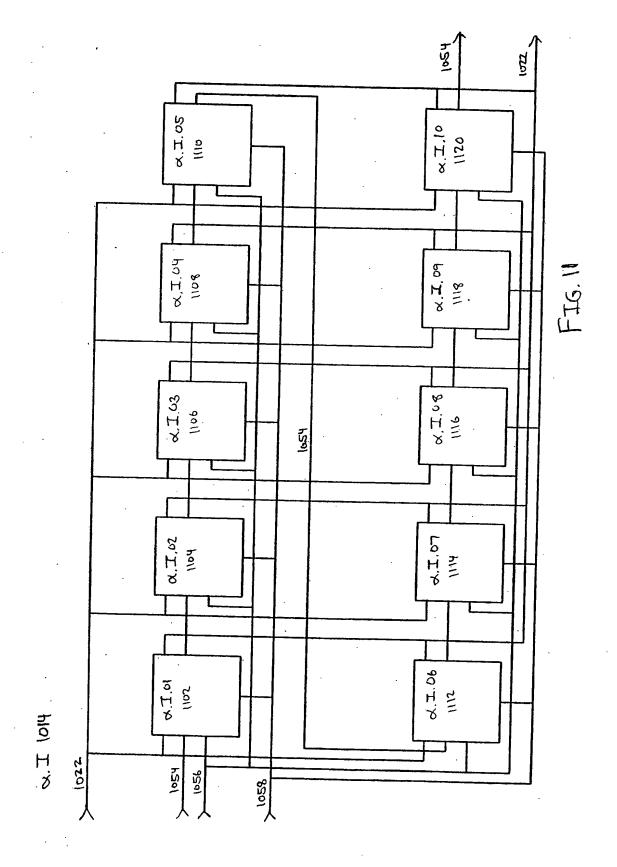
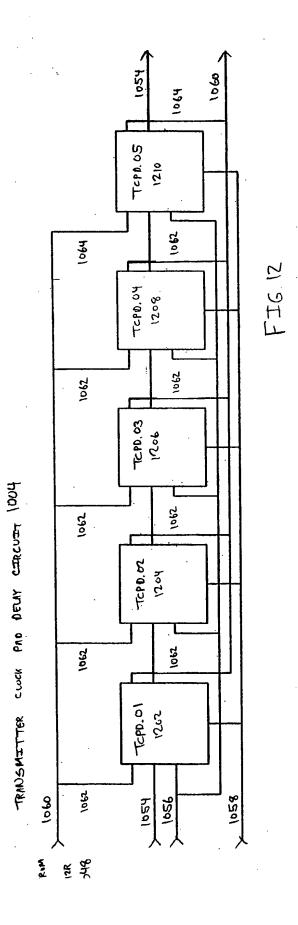
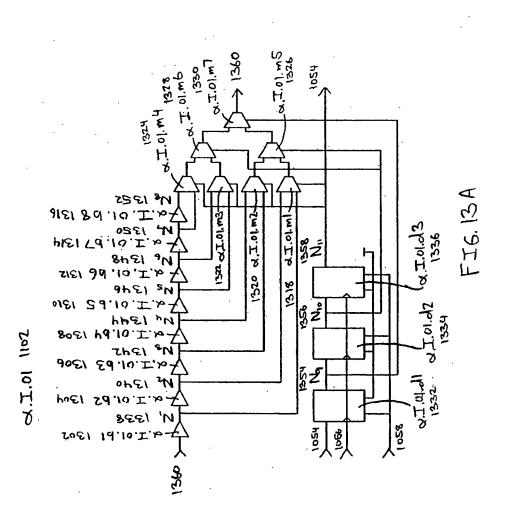


FIG. 9









Output

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FIG. 13B \3-80 ź

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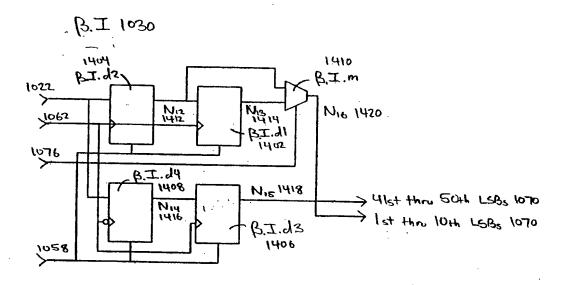


FIG. 14

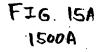
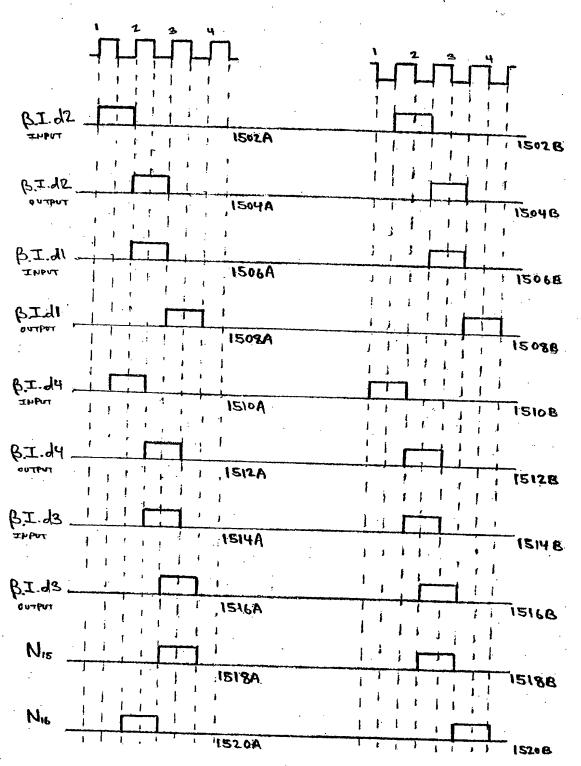


FIG. 158



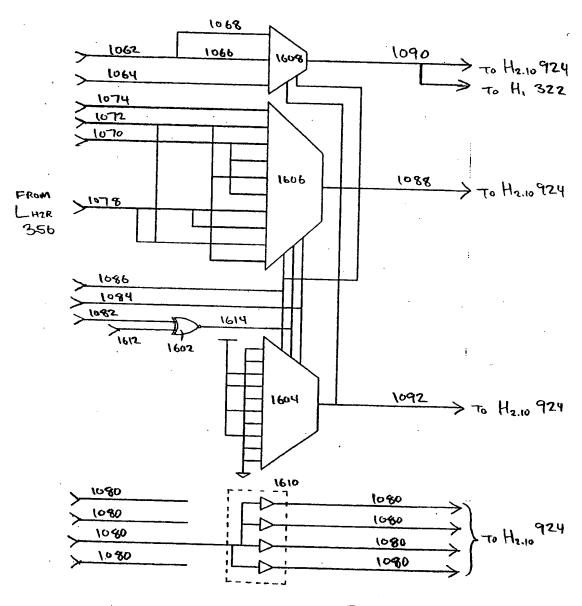
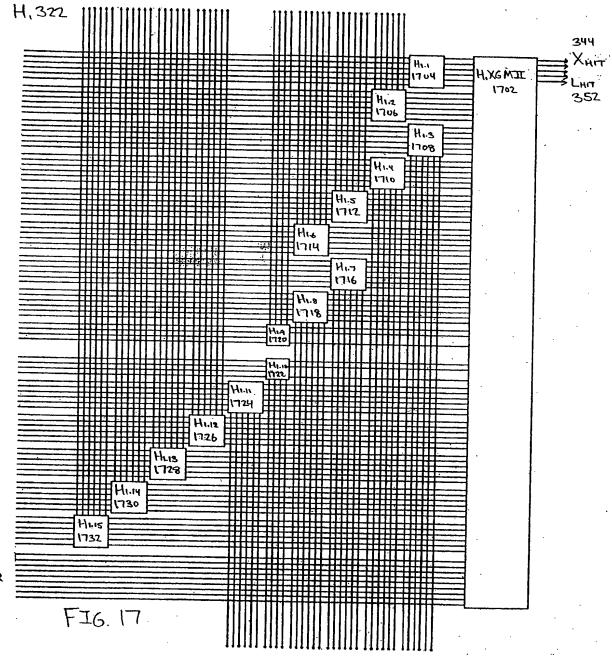
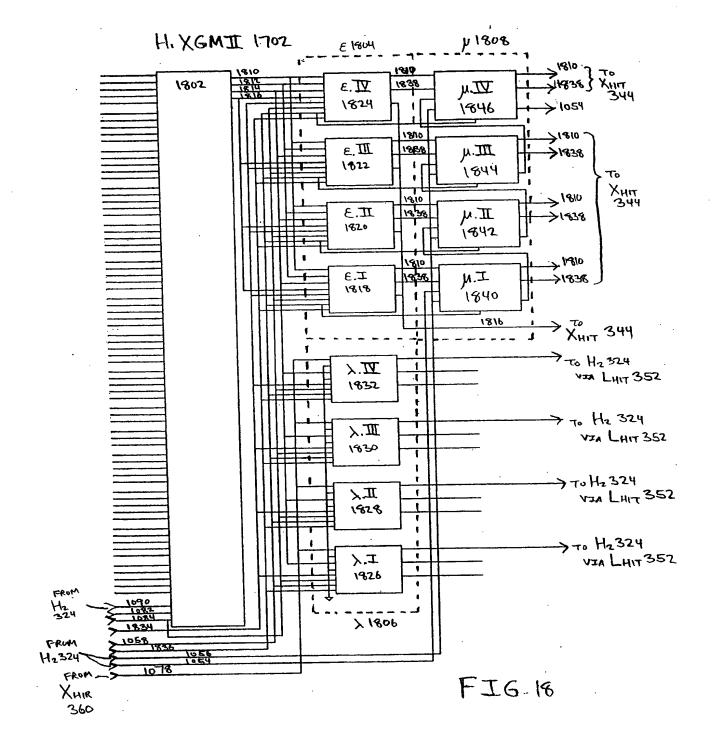


FIG. 16



XHIR 360



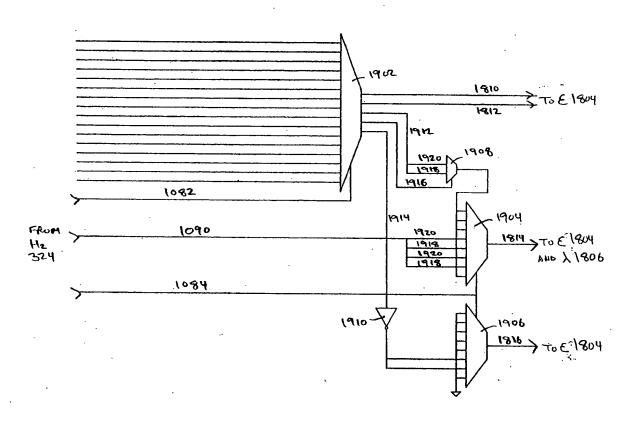
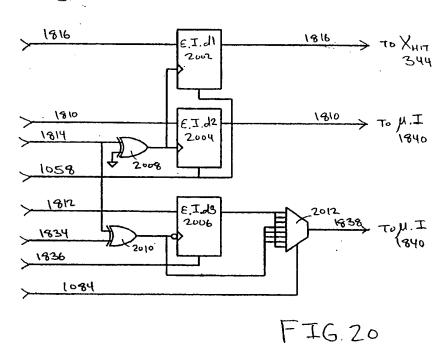
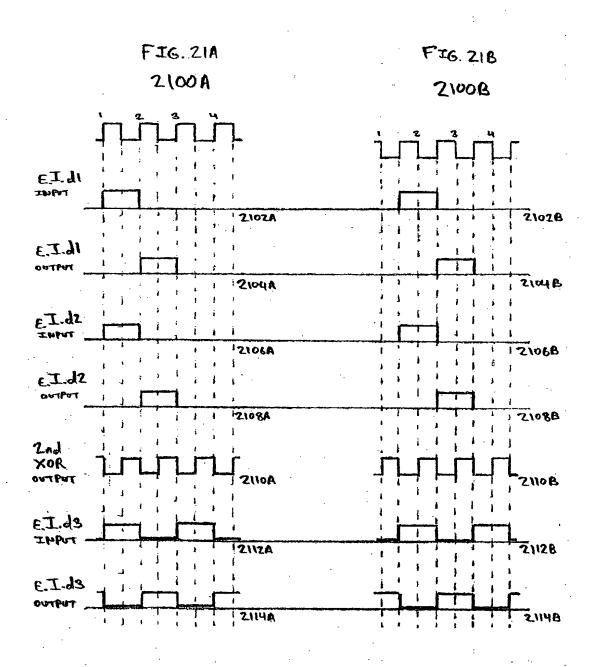
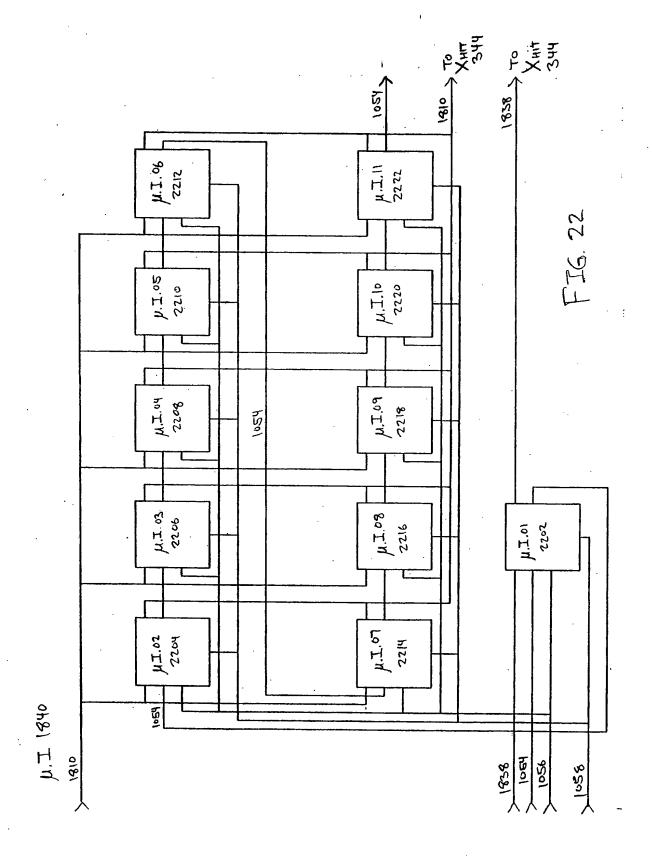


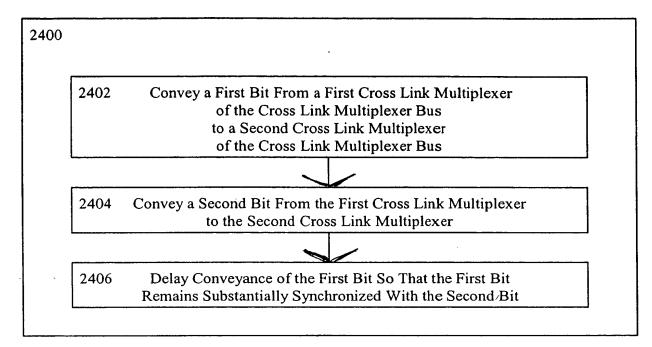
FIG. 19

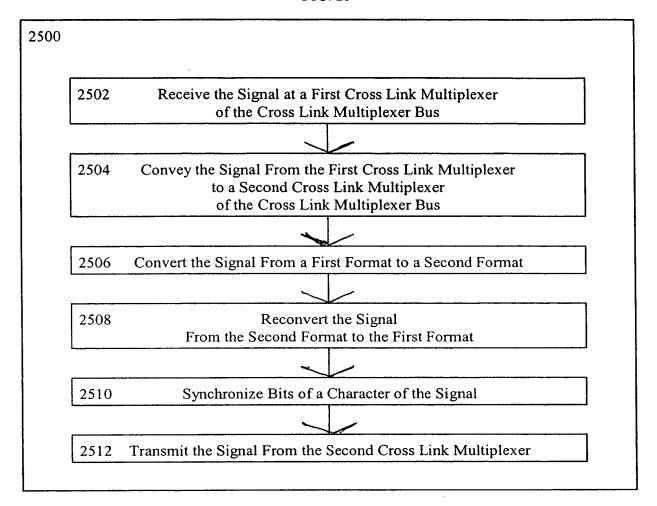






2302	Receive the Signal at a First Cross Link Multiplexer of the Cross Link Multiplexer Bus
2304	Convey the Signal From the First Cross Link Multiplexer in a First Direction Toward a Second Cross Link Multiplexer of the Cross Link Multiplexer Bus
2306	Convey the Signal From the First Cross Link Multiplexer in a Second Direction Toward the Second Cross Link Multiplexer
2308	Receive the Signal From the First Cross Link Multiplexer in the First Direction at a Third Cross Link Multiplexer of the Cross Link Multiplexer Bus
2310	Convey the Signal From the Third Cross Link Multiplexer in the First Direction Toward the Second Cross Link Multiplexer
2312	Receive the Signal at the Second Cross Link Multiplexer From a Third Cross Link Multiplexer of the Cross Link Multiplexer Bus





2602	During a First Cycle of a Clock, Convey a First Character From an Input of a First Interconnect	
	to an Output of the First Interconnect	
2604	During the First Cycle of the Clock, Convey the First Character From an Input of a Second Interconnect to a Delay Flip-Flop	
2606	During a Second Cycle of the Clock, Convey the Second Character From the Input of the First Interconnect to the Output of the First Interconnect	
2608	During the Second Cycle of the Clock, Convey the First Character From the Delay Flip-Flop to an Output of the Second Interconnect	

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	Determine a First Time for the First Bit to Be Conveyed	
	Via a First Interconnect	
	From a First Cross Link Multiplexer to a Second Cross Link Multiplexer	
	When a First Series of Delay Buffers Is Bypassed	
2704	Determine a Second Time for the Second Bit to Be	
	Conveyed Via a Second Interconnect	
	From the First Cross Link Multiplexer	
	to the Second Cross Link Multiplexer	
	When a Second Series of Delay Buffers Is Bypassed	
2706	Determine a Desired Delay Time for the First Bit	
	So That the First Bit Is Synchronized With the Second Bit	
· ',		
2708	Align the First Series of Delay Buffers	
	to Increase the First Time by the Desired Delay Time	

2802	Convey a First Bit of a Character of a Signal
	Through a First Interconnect
	of the Plurality of Substantially Parallel Interconnects
2804	Convey a Second Bit of the Character of the Signal
	Through a Second Interconnect
	of the Plurality of Substantially Parallel Interconnects
2806	Convey a Power Supply Voltage
	Through a Third Interconnect
	of the Plurality of Substantially Parallel Interconnects

2902	Convey a First Data Bit of a Character of a Signal
	Through a First Interconnect
	of the Plurality of Substantially Parallel Interconnects
2904	Convey a Second Data Bit of the Character of the Signal
	Through a Second Interconnect
	of the Plurality of Substantially Parallel Interconnects
2906	Convey a Control Bit of the Character of the Signal
	Through a Third Interconnect
	of the Plurality of Substantially Parallel Interconnects